**Remarks**

Claims 1 - 4 and 6 - 11 are in the application. Reconsideration of the application is requested, in view of the following Remarks.

Generally, a chip scale package has an integrated circuit die mounted on, and electrically connected to, a substrate. The package is ordinarily installed for use by mounting the package on a printed circuit board. Electrical connection between the package and the circuit board "second level interconnection" may be made by way of solder balls that are attached to the package substrate and reflowed onto connection sites on the printed circuit board. (*See*, Applicants' page 1, paragraph [0005], particularly lines 24 - 25; page 4, paragraph [0025], particularly lines 12 - 13.)

Applicants' invention is directed to chip packages employing solid-state flip chip interconnection between the die and the package substrate, and having the die mounted on the same side of the substrate as the solder balls for second level interconnection to the printed circuit board. (*See*, page 2, paragraph [0008].) Solid-state flip chip interconnection of the die to the substrate provides for a very thin package; and because the die and the second level interconnect balls are attached on the same side of the substrate, the effective thickness of the die is accommodated within the second level interconnect gap, and contributes nothing to the overall package thickness. (*See*, paragraph [0010], particularly lines 19 - 21.)

The specific points raised by the Examiner will now be addressed, beginning with the rejections under 35 U.S.C. §102.

Rejections under 35 U.S.C. § 102(b)

Claims 1 - 4 and 6 - 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by "David et al. (Japan Patent # 2000-156457)". The Examiner asserted that:

> David et al. (figures 1 to 3) specifically figure 3 show a chip scale integrated circuit chip package comprising a die 10 mounted by flip chip interconnection to a first surface of a package substrate 14, wherein the flip chip interconnection comprises solid state connections (see the abstract's solution section) of interconnect bumps 18 affixed to the die with interconnect pads 12 on the first

> surface of the substrate, and second level interconnections 16 formed on the first surface of the package substrate.

This rejection is traversed. Applicants, respectfully, disagree with the Examiner's reading of Japan patent publication JP 2000-156457. JP 2000-156457 discloses nothing regarding second level interconnection of a **package** onto a **circuit board**, and the features 16 in JP 2000-156457 have nothing whatever to do with second level interconnections between a package and a circuit board.

Japan patent publication JP 2000-156457 claims priority from U.S. Application No. 109655 (*See*, items (33), (31) on the cover sheet of JP 2000-156457). Applicants have obtained a copy of U.S. 5,897,341 ("Love '341"), which issued from U.S. Application No. 09/109,655, and a copy of Love '341 is being disclosed in a supplemental information disclosure statement submitted herewith.

Applicants' claims recite second level interconnections formed on the same surface of the package substrate as the flip chip mounted die. JP 2000-156457 [also Love '341] does not teach anything regarding second level interconnection; even less does it teach or suggest mounting the die and the second level interconnections on the same side of the package substrate as in Applicants' invention as claimed and, accordingly, the rejections for anticipation by JP 2000-156457 should be withdrawn.

Claims 1 - 4 and 6 - 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Maeta *et al.* U.S. 5,677,246 ("Maeta"). The Examiner asserted that:

> Maeta et al. (figures 1B to 18B) specifically figure 11 show a chip scale integrated circuit chip package comprising a die 2 mounted by flip chip interconnection to a first surface of the package substrate 1, wherein the flip chip interconnection comprises solid state connections (see column 12, lines 45 - 53) of interconnect bumps 1b affixed to the die with interconnect pads 2a on the first surface of the substrate, and second level interconnections 1a formed on the first surface of the package substrate.

This rejection is traversed. Applicants, respectfully, disagree with the Examiner's reading of Maeta. Maeta states, for example, with reference to FIG. 3B:

> The semiconductor device comprises a wiring substrate 1 having the wiring 1a containing a connection section 1b on one major surface, a semiconductor chip 2 mounted with the face down on one major surface of the substrate, a resin layer 5 filled and hardened between the chip and the substrate, an external connection terminal 4 formed on the other major surface of the substrate, and a contact conducting wiring 3 formed within a through-hole in the substrate 1 and connecting the wiring 1a to the external connection terminal 4.

(Maeta Col. 8, lines 47 - 54; *see also*, Maeta Col. 1, lines 48 - 60, referring to Maeta FIG. 16.) The features 1a in Maeta have nothing whatever to do with second level interconnections between a package and a circuit board. Second level interconnection of the package described in Maeta would be made by way of the so-called "external connection terminal 4", which is everywhere in Maeta shown as being on the side of the substrate 1 opposite the side on which the semiconductor chip 2 is attached ("the other major surface of the substrate"). Vias through the substrate are required in Maeta for connection of the die-interconnect circuitry (1a) with the second level interconnection (4). (*See*, Maeta Figs. 3B, 10A, 11, 13A, 16, 17).

Maeta does not describe mounting the die and the second level interconnections on the same side of the package substrate as in Applicants' invention as claimed (to the contrary, Maeta describes the external connection terminals as being on the opposite side) and, accordingly, the rejections for anticipation by Maeta should be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 1 - 4, 6 - 9 and 11 were rejected under 35 U.S.C. § 103(a) for obviousness over Rolda, Jr., US 2002/0030261 A1 ("Rolda") in view of "David et al. (Japan Patent # 2000-156457)". JP 2000-156457 is applied as in the rejections under Section 102(b). As to Rolda the Examiner acknowledged that:

> Rolda, Jr. et al. fail to explicitly show the flip chip interconnection comprises solid state connections of interconnection bumps affixed to the die with interconnection pads on the first surface of the substrate.

And the Examiner argues that it would have been obvious "to use solid state connection as a design choice."

This rejection is traversed. Not only does Rolda fail to suggest (much less describe) solid state flip chip interconnection; Rolda everywhere expressly describes interconnection by solder reflow. (In fact, Rolda describes the interposer as preferably being made of a compliant material to provide a stress buffer to relieve some of the strain that develops in the chip solder balls in thermal cycling. *See*, Rolda paragraph [0036].) Accordingly, to the extent Rolda may be relevant, it teaches away from Applicants' invention.

The Examiner does not point to any motivation in the art for making the proposed combination, and the combination proposed by the Examiner is a product of hindsight, informed by Applicants' disclosure. That is an improper basis for an obviousness rejection and, accordingly, the rejection for obviousness over Rolda and JP 2000-156457 should be withdrawn.

Claims 1 - 4 and 6 - 10 were rejected under 35 U.S.C. § 103(a) for obviousness over Inaba *et al.* U.S. 6,166,443 ("Inaba") in view of "David et al. (Japan Patent # 2000-156457)". JP 2000-156457 is applied as in the rejections under Section 102(b). As to Inaba the Examiner acknowledged that:

> Inaba et al. fail to explicitly show the flip chip interconnection comprises solid state connections of interconnection bumps affixed to the die with interconnection pads on the first surface of the substrate.

And the Examiner argues that it would have been obvious "to use solid state connection as a design choice."

This rejection is traversed. Not only does Inaba fail to suggest (much less describe) solid state flip chip interconnection; Inaba everywhere expressly describes interconnection by solder reflow. Accordingly, to the extent Inaba may be relevant, it teaches away from Applicants' invention.

The Examiner does not point to any motivation in the art for making the proposed combination, and the combination proposed by the Examiner is a product of hindsight, informed by Applicants' disclosure. That is an improper basis for an obviousness rejection and, accordingly, the rejection for obviousness over Inaba and JP 2000-156457 should be withdrawn.

In view of the foregoing, it is believed that all the claims in the application are in condition for allowance, and action to that effect is requested.

This response is being filed within the shortened statutory period set by the Examiner and, accordingly, it is believed that no extension of time or fee therefor is required in connection with this paper.

This response is accompanied by a Notice of Appeal, and a fee therefor.

This response is also accompanied by a Supplemental Information Disclosure Statement, disclosing the U.S. counterpart of the JP patent publication cited by the Examiner in the Office action; the Supplemental IDS is accompanied by an appropriate fee.

If the Examiner determines that a further extension of time is required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge the fee to Deposit Account 50-0869 (Order No. CPAC 1010-2).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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